Estimating PLL Bandwidth, Jitter Transfer & Period Jitter from Phase Noise Plots

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Once every few years almost all of the well-established high frequency serial communication standards (PCI-Express, USB, Ethernet, SONET, SATA, Infiniband, etc.) are revised in order to better cope with the greater expectations of our data hungry society. As new versions of these standards are introduced, the demands placed on the electronic circuitry supporting them are heightened. High performance clock generation and distribution devices incorporated into modern system implementations use frequency domain parameters, namely phase noise and phase jitter, to describe their performance. The following article discusses how a phase noise plot allows the estimation of clock device characteristics that are not explicitly mentioned on the manufacturer’s datasheet, so that engineers can make a better assessment of its suitability for a particular application.

When implementing a high speed serial link, period jitter can be utilized to derive the bit error rate (BER) involved. Jitter transfer and PLL bandwidth of a clock device are also important metrics, as through these it will be possible to better fathom how the input source or input clock will affect the output of the device. All of these will help the engineer to select the right clock device to meet their needs. Nevertheless, it is rare that they are directly cited, so calculations must be made instead.

**Jitter Transfer**

Jitter transfer gives the amount of attenuation or noise generation over a range of offset frequencies. This is defined by the loop filter response of the PLL. A phase noise plot provides the noise density at all offset frequencies, so it contains the requisite data for determining the clock device’s jitter transfer. The best way to show jitter transfer, generation and attenuation, is to use a source with a higher noise floor at lower offset frequencies and lower noise floor at higher offset frequencies. At low frequencies, the PLL will pass high source noise to the output and at high frequencies it will show its intrinsic noise floor, this is due to a low pass bandwidth nature of a PLL.

A low bandwidth PLL can attenuate jitter even at lower offset frequencies and the lower the PLL bandwidth, the better the attenuation will be at such frequencies. However, low bandwidth PLLs have the drawback of slower response time - taking time to track input clock changes.
Most networking communication links have less stringent constraints at lower offset frequencies.

**PLL Bandwidth**

In addition to jitter transfer, a phase noise plot can also help to determine PLL bandwidth provided an appropriate reference clock source is utilized. To fully understand PLL bandwidth estimation and the jitter transfer of a PLL, a simple measurement set up should be undertaken, with two different clock sources fed into a high performance zero delay buffer (ZDB).

A simple schematic describing the phase noise measurement setup is shown in Figure.1. The measuring is carried out using an Agilent 5052A signal source analyzer. Both the Source-1 (a high performance clock generator) and the ZDB are powered by a low noise power supply.
As shown in Figure.2, the Source-1 has root mean square (RMS) phase jitter of ~447fs, where the buffered output has ~448.8fs. The RMS jitter is measured over offset frequencies from 10kHz to 20MHz. At lower offset frequencies, 10-100Hz, the buffer noise is high compared to the source, but this is not a concern for most communication channels as it is easily tracked by the PLLs. The output buffer plot approximately matches the source plot up to 1MHz. Hence, the buffer PLL bandwidth can be estimated at around 1MHz. Above this frequency the buffer output has a lower noise floor than the source, as highlighted by circle-2 in Figure.2.

A data pattern generator (DPG) is employed for Source-2. It has a higher noise floor than Source-1. Hence, the buffered output plot shown in Figure.3 matches the input source plot at lower frequencies (10-100Hz). The buffer-PLL transfers the input noise below 1MHz; the abrupt variation around 30kHz in the source noise plot is reflected in the buffer output noise plot, highlighted in circle-1 of Figure.3. For frequencies above 1MHz, the buffer noise floor is evidently lower compared to the source, as pointed out by circle-2 in Figure.3; this indicates that the buffer acts as jitter attenuator in this frequency range.
Figure 3: Phase noise plot of Source-2 & buffered output

**Period Jitter**

As already mentioned, period jitter is an important parameter for BER approximation in high speed serial standards, but normally only phase jitter or phase noise data measured using low noise frequency domain equipment is provide by clock device manufacturers. The phase noise spectrum is defined as attenuation in dB/Hz from the peak value of carrier power spectral density. The relation between phase noise spectral density and RMS period jitter is:

\[
\Delta t^2_{RMS} = \frac{T_c^2}{4\pi^2} \int_{0}^{\infty} S\phi(f) \times 4 \times \sin^2(\pi f \tau) \, df
\]

Equation 1

The conversion factor \( \frac{T_c^2}{4\pi^2} \) translates jitter from radians into seconds. For jitter measurements, \( \tau \equiv T_c \). Here, \( S\phi(f) \) is total noise power spectral density, which can be related to \( L(f) \) (phase noise at offset frequency) as shown below:

\[ S\phi(f) \approx 2 \times L(f) \]
\[ \Delta t_{RMS}^2 = 2 \left[ \frac{T_c^2}{4\pi^2} \int_0^\infty L(f) \times 4 \times \sin^2(\pi f_T) \, df \right] \]

\[ \Delta t_{RMS}^2 = \Delta t_{rms,PN}^2 + \Delta t_{rms,Spur}^2 \]

Equation 2

To estimate the period jitter from a phase noise plot, the phase noise at offset frequencies must be multiplied by the \(4\sin^2(\pi f_T)\) function. The dB conversion \(4\sin^2(\pi f_T)\) shows that it has -20dB/decade slope (see Figure 5). The \(4\sin^2(\pi f_T)\) values in dB can be added to phase noise plot data in dBc. The numerical integration of the resulting data over the offset frequency range of interest will provide the phase noise density in single side band. By way of an example, to estimate period jitter from the phase noise plot given in Figure 4, add the \(4 \sin^2(\pi f_T)\) function data in dB to the PN data (dBc/Hz) as shown in Figure 5. The resulting blue curve shows the phase noise spectral density.

**Figure 4**: Clock generator output PN plot with spurs
Figure 5: Phase noise spectral density at 100 MHz carrier

Integration of the area under the blue curve in Figure 5 will give the phase noise spectral density in dB (denoted as area A). This can be converted into RMS jitter using the following equation:

$$RMS\ Jitter(\text{seconds}) = \sqrt{\frac{\Delta t_{rms}^2}{A}} = \frac{T_c}{2\pi} \left( \sqrt{2 \times 10^4/10} \right)$$

Equation 3
Figure 6: RMS jitter conversion from phase noise

As shown in Figure 6, the area under the curve can be divided into multiple sections (A1, A2, etc.) as per the shape of the curve or using a piecewise linear function. Since lower offset frequency noise does not contribute significantly to the period jitter, only the curve under higher offset frequencies is considered. For better accuracy, the entire curve can be divided into multiple sections and each section’s impact on period jitter gauged. The curve in Figure 6 is divided into four sections, with two corresponding data points (phase noise, offset frequency) per section. Using these data points, each section area can be converted into equivalent jitter (expressed in seconds).

Each section’s contribution to RMS jitter is shown in Figure 6. The sum of these RMS jitter values can be calculated using the following equation:

\[ \Delta t_{rms}^2 = \Delta t_{rms}^2 A_1 + \Delta t_{rms}^2 A_2 + \ldots + \Delta t_{rms}^2 A_N \]

Equation 4

From this equation, the total jitter contribution of the four areas displayed in Figure 6 is summed with 434 fs, \( \Delta t_{rms} A \). This is multiplied by 2 to give the total noise contribution, 868 fs, \( \Delta t_{rms PN} \). Apart from this there are two spurs appearing in Figure 6. As these spurs are on single frequencies, their contribution to jitter can be calculated separately and added through the following equation:

\[ \Delta t_{rms, spur}^2 = \Delta t_{rms, sp_1}^2 + \Delta t_{rms, sp_2}^2 + \ldots + \Delta t_{rms, sp_N}^2 \]

Equation 5
\[ \Delta t_{rms,sp,n}^2 = \left[ \frac{T_0^2}{4\pi^2} \left( L(f_n) \times 4 \times \sin^2(\pi f_n \tau) \right) \right] \]

Each spur’s dB value can be converted into jitter using Equation.3.

The example shown in Figure.6 has two spurs at frequencies 1.4MHz and 25MHz of -111dB and -72.6dB respectively. The RMS jitter equivalent of the 1.4MHz spur is 6.3fs and the 25MHz spur is 527fs. Spurs at higher frequencies will have greater impact on period jitter than lower frequency spurs. The 25MHz spur is of much higher value than the 1.4MHz spur. The total spur RMS jitter value, using Equation.5, is very close to 527fs, \( \Delta t_{rms,spur} \), hence the 1.4MHz spur’s impact can be regarded as negligible. High dB spurs can be error prone in certain applications due to their increased jitter impact. Using Equation.2, the total period jitter of the plot described in Figure.6 is estimated at 1.015ps.

In conclusion, frequency domain parameters, such as phase noise and phase jitter, are of great value to engineers when specifying a clock device. The phase noise plots provided by device manufacturers act as a vital performance indicator for these products. A plot can be used to approximate bandwidth and jitter transfer characteristics for the PLL, thereby helping determine its behavior (as a jitter attenuator or generator) in the relevant frequency range. Period jitter can also be estimated from a given plot, by considering the phase noise of the dominant frequency range and the spurs at critical frequencies. Using this information engineers looking to specify clock devices for their next generation design implementations can make product selection decisions with a greater degree of authority.